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**Evariste III**: A new multi-FPGA system for fair benchmarking of hardware dependent cryptographic primitives

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**What’s new?**
- 3 new FPGA modules, one with an embedded ARM processor
- Motherboard with ZIF (zero insertion force) connectors
- Serial connection of up to 6 modules via JTAG
- Box with 6 motherboards interconnected and chained
- 30 modules of each new FPGA family for PUF evaluation available
- SMA connectors in all modules for side channel analysis added

**Inherited from Evariste II**
- Both scripting and fast acquisition data programs
- Open source system
- Remotely available via Internet
- Fast USB interface

**TRNGs**
System dedicated to True Random Number Generators

**PUFs**
System dedicated to Physical Unclonable Functions

**SCAs**
System dedicated to Side Channel Analyses

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