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**Evariste III**: A new multi-FPGA system for fair benchmarking of hardware dependent cryptographic primitives

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**What’s new?**
- 3 new FPGA modules, one with an embedded ARM processor
- Motherboard with ZIF (zero insertion force) connectors
- Serial connection of up to 6 modules via JTAG
- Box with 6 motherboards interconnected and chained
- 30 modules of each new FPGA family for PUF evaluation available
- SMA connectors in all modules for side channel analysis added

**Inherited from Evariste II**
- Both scripting and fast acquisition data programs
- Open source system
- Remotely available via Internet
- Fast USB interface

**TRNGs**
System dedicated to True Random Number Generators

**PUFs**
System dedicated to Physical Unclonable Functions

**SCAs**
System dedicated to Side Channel Analyses

**3 new modules:**
- New motherboard
  - ZIF connectors
  - JTAG chain I/O
- Xilinx Spartan 6
- Altera Cyclone V
- Microsemi SmartFusion2 with ARM Cortex-M3

**Compatible with old modules:**
1. Xilinx Spartan 3
2. Xilinx Virtex V
3. Altera Cyclone III (3 versions)
4. Altera Aria II
5. Microsemi Fusion (2 versions)
6. ASIC controlled with Fusion FPGA

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NATO SFP (Science for Peace) 2013: SFP-984525 “Secure implementation of post-quantum cryptography”.

« An open-source multi-FPGA modular system for fair benchmarking of true random number generators »,
3rd international conference on field programmable logic and applications (FPL2013), pp. F53_R, Porto, Portugal

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1. FISCHER V., HADDAD P., BERNARD F. [2013]:
"An open-source multi-FPGA modular system for fair benchmarking of true random number generators",
3rd international conference on field programmable logic and applications (FPL2013), pp. F53_R, Porto, Portugal