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# Predictability and impact of product layout induced topology on across-field focus control

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## Abstract:

With continuing dimension shrinkage using the TWINSCAN NXT:1950i scanner on the 28nm node and beyond, the imaging depth of focus (DOF) becomes more critical. Focus budget breakdown studies [Ref 1, 5] show that even though the intrafield component stays the same this becomes a larger relative percentage of the overall DOF. Process induced topography along with reduced Process Window can lead to yield limitations and defectivity issues on the wafer. To improve focus margin, a study has been started to determine if some correlations between scanner levelling performance, product layout and topography can be observed. Both topography and levelling intrafield fingerprints show a large systematic component that seems to be product related. In particular, scanner levelling measurement maps present a lot of similarities with the layout of the product. The present paper investigates the possibility to model the level sensor's measured height as a function of layer design densities or perimeter data of the product. As one component of the systematics from the level sensor measurements is process induced topography due to previous deposition, etching and CMP, several layer density parameters were extracted from the GDS's. These were combined through a multiple variable analysis (PLS: Partial Least Square regression) to determine the weighting of each layer and each parameter. Current work shows very promising results using this methodology, with description quality up to 0.8  $R^2$  and expected prediction quality up to 0.78  $Q^2$ . Since product layout drives some intrafield focus component it is also important to be able to assess intrafield focus uniformity from post processing. This has been done through a hyper dense focus map experiment which is presented in this paper.

**Keywords:** depth of focus, intrafield, scanner levelling, topography, scanner, product design layout effect, PLS regression analysis

## INTRODUCTION

For low  $k_1$  lithography, the scanner control capabilities are very similar to the process window of critical features so that process margin is drastically reduced. In early phase of technology development TWINSCAN NXT:1950i focus budget breakdown shows values that are sometimes larger than the depth of focus of some critical patterns within the chip. In this scope, bringing process to maturity requires actions to retrieve appropriate process margin to secure the yield. Some of these actions will address random dynamic behaviour of the scanner while others will focus on systematic fingerprint and their mitigation.

The depth of focus can be enhanced or controlled using a number of different methods.

- Process window enhancement (Mask3D/Resist3D aware OPC, SMO, etc.)
- Feature to feature Best Focus shift mitigation through mask enhancement (mask blank)
- Precision and accuracy gains for Best Focus determination using new methods
- In-line monitoring
- Topography compensation (Design for Manufacturing, other processes)
- Levelling control (TWISCN NXT:1970Ci, UV-LS, AGILE2)
- Interfield focus control (BaseLiner Focus, Field Width Optimized Levelling, Chuck Deformation Map updating, Imaging Optimizer)
- Layout (or hotspot) aware scanner control( Process Window Optimizer)

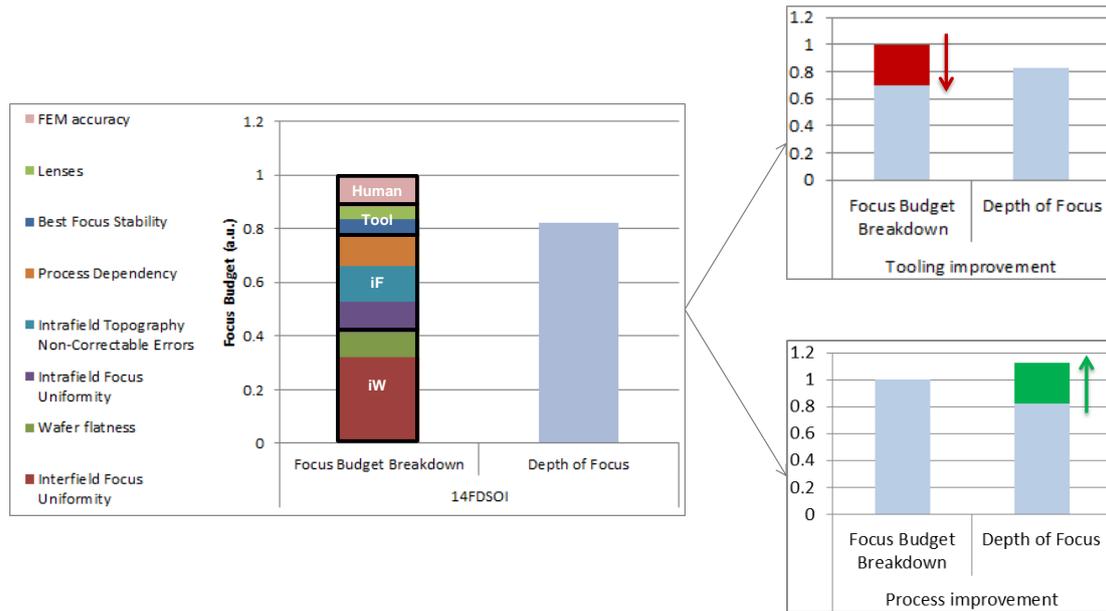


Figure 1: Scanner focus budget breakdown vs. process DOF of the studied reference pattern for the 14FDSOI technology

Figure 1 shows the current focus budget breakdown for 14FDSOI versus the depth of focus of the process at Contact layer [Ref 1]. Intrafield and interfield focus components count together for more than 2/3 of the total budget for both 28 and 14FDSOI technologies.

This paper will look into the topological and levelling component of the focus budget.

## I – SCANNER LEVELLING FLOW

During the lithographic exposure processes, it is important to ensure that the mask image is correctly focused on the dies in the wafer. For this correct positioning of the wafer, levelling is used in the lithographic tools. Levelling can be referred to as the process of measuring the 'vertical' position of the wafer by a Level Sensor (LS) and using this information to keep the wafer in (best) focus during exposure. Level Sensor is an optical interferometric sensor that measures the surface height using optical triangulation method. From the level sensor measurement, a 'wafer map' containing the surface height of the wafer placed on a wafer stage is created.

Figure 2 shows a wafer map. A wafer map can be divided into multiple areas corresponding to dies or fields. After subtracting the global shape from the wafer map, an average height map of the fields are then calculated and shown in figure 2 (right). The latter is representative of the intra field topography measured by the level sensor (LS).

Level sensors used for the wafer map measurements can be subject to process dependency [Ref 6]. Process dependency is a form of measurement error in which level sensor provide differing results depending on how the measured wafer has previously been processed. For example, a level sensor may provide a particular height measurement for a wafer including a silicon substrate coated with a single layer of resist, and may provide a different height measurement for a wafer including a silicon substrate coated with several layers of resist, even if both wafers' surface are at the same actual height.

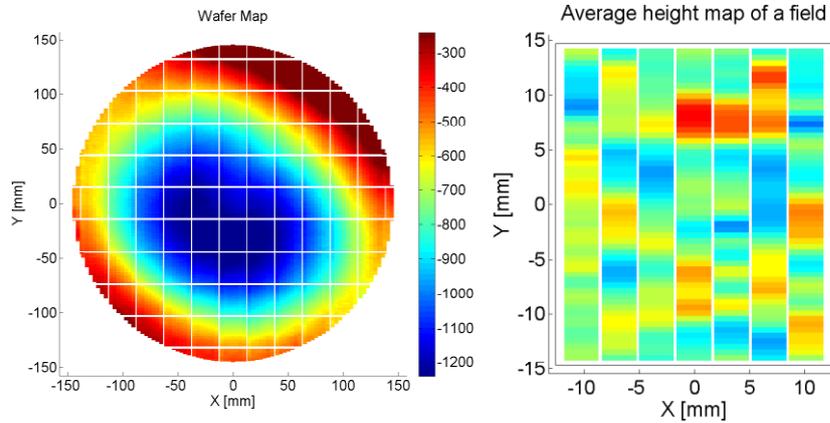


Figure 2: (Left) Level sensor measured wafer surface height map and (Right) average height map of a field (die) of the wafer.

One error caused by process dependency is referred to as process dependent apparent surface depression, and is understood to be caused by an optical effect known as the Goos-Haenchen shift [Ref 7]. The Goos-Haenchen shift is a lateral translation of light along a reflecting surface (in this case the resist) during reflection. The shift is dependent upon the material and layer structure of the substrate and is due to the visible light used by the Level Sensor. The newest scanner generation has a level sensor using UV light suffering less from this effect.

$$LS = Actual\ topography + Process\ dependency \quad (1)$$

As a result of process dependency, a die may not be correctly located in the focal plane of the projection lens. To overcome this, process dependency corrections are applied to the level sensor measured wafer map. ASML's commercial products 'Air Gauge (AG)' and 'AGILE (Air Gauge Improved Levelling)' is used to do this correction. So, the process dependency corrected intra field height map is more accurate measurement of the intra field topography.

$$LS_{AGcorrected} = LS - Process\ Dependency\ Correction \approx Actual\ Topography \quad (2)$$

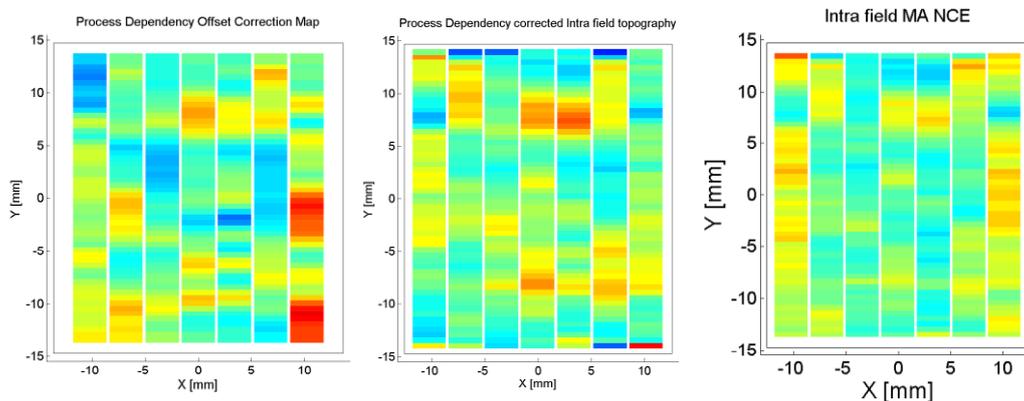


Figure 3: (Left) Process dependency correction, (Middle) process dependency corrected intra field topography map and (Right) intra field levelling MA NCE

The wafer map is used to derive setpoints to actuate the wafer stage to position the dies in focus at the location where the projection takes place. Due to the finite size and rectangular nature of the exposure slit, some of the surface topography cannot be leveled completely. This non-level-able residual is called non-correctable errors (NCE). During a scanned exposure, the non-correctable errors change continuously as the slit is scanned over a particular position on the wafer. In the latter case, the average value of the non-correctable errors over exposure time, defines the average defocus that this position experiences. This average value is termed as the moving average of the non-correctable errors (MA-NCE). Topography changes that are smoother than the slit dimensions can be leveled by adjusting the stage height and tilt angle accordingly. If the topography varies within the slit dimensions, the height changes cannot be leveled effectively. Hence, a large part of the highly variant topography is non correctable and is often present in the MA NCE map.

## II – METHODOLOGY / CONCEPT

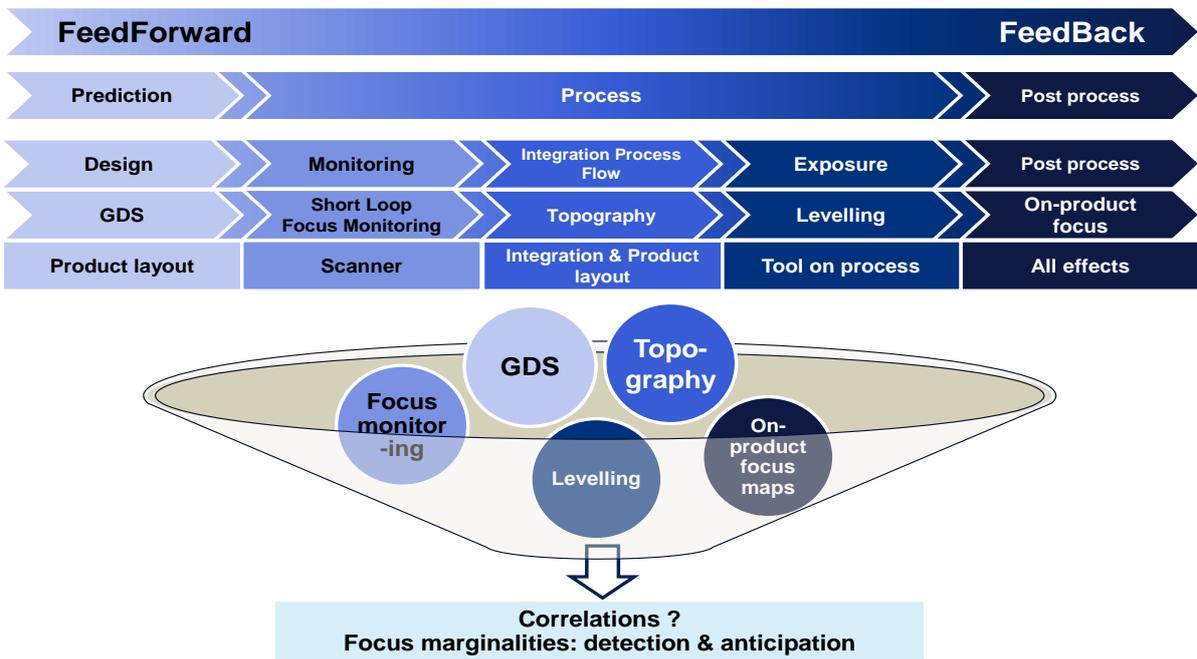


Figure 4: Different data sources and their use in the focus correlation study (GDS: Design layout, Short loop focus monitoring: Single Shot Focal test, On-product focus: Focus Uniformity Map “Bossung top best focus”)

The study that is initiated in this paper consists of a multi-source data analysis. Inputs include scanner log files, GDS’s, on-product and bare-wafer focus and topography measurements. They are processed together in a multivariate analysis tooling (Partial Least square regression software) in order to generate a prediction model. Figure 4 above summarizes the different sources of data and their availability in the manufacturing flow.

### 1. GDS extracted data

It is possible to generate layer density and perimeter files directly from the product GDS. Density and perimeter data are extracted at both a millimetre and micrometre scale to match the scanner reports, the focus uniformity maps and the topography measurements layouts. Density maps correspond to spatial density of patterns, i.e. to the density of top surface of patterns for a given area. The extracted perimeter data is the density of sidewall of patterns for a given area. Both density and perimeter influence the material distribution, which has some impact on the optical modulation that the level sensor is suffering from (Level Sensor Process Dependency), and process induced topography interfield and

intrafield (previous CMP and deposition steps). This data can be used to generate a high density map of wafer topography, which may be used as one of the inputs for Process Window Optimizer.

## **2. Scanner reports**

These logs are automatically generated for every lot that is processed on the scanner. The levelling part of the report contains information on the wafer topology at a millimetre resolution for every wafer in the lot. Data that can be extracted from these files are the following:

- Optical Level Sensor raw maps
- Process Dependency corrected LS maps
- Process Dependency maps of the LS
- Non-correctable errors (NCE) maps

## **3. Focus uniformity mappings**

Interfield and intrafield focus maps are measured by CDSEM at 52 locations across field on product exposures. This was done by measuring CD on 7 product wafers with 15nm focus steps between each wafer. A Bossung was then reconstructed at each measurement location and the Bossung top was taken as the best focus position. These exposures were done on a TWINSCAN NXT:1950i with AGILE enabled and Baseline Focus disabled. An inline alternative to this technique is on-product intrafield and interfield focus measurements using ASML's uDBF targets.

## **4. Topography measurements**

Intrafield and interfield topography measurements can be performed at micrometre resolution using multiple different offline optical measurement tools [Ref 4]. This gives high frequency topography maps that the scanner cannot measure due to the resolution of the level sensor and AirGauge sensor. With this extra information it will be possible to perform a 1 time verification of the results from the GDS density design analysis and use the data for optimizing scanner focus control. Note that for this paper, these data are not yet fully available and analysed.

## **5. Short loop focus monitoring**

The Single Shot Focal test was exposed with 13x19 FOCAL marks per field on a bare silicon wafer with the same field layout as the product wafers. This was measured using the scanners alignment sensor to give the interfield scanner focus fingerprint. The test was executed on a TWINSCAN NXT:1950i with AGILE enabled and without Baseline Focus correction (which is used to correct for the scanner fingerprint in production). This means that the SSF fingerprint contains correctable errors as well as scanner non-correctable errors.

## 6. Inputs summary

INPUT N°	INPUT NAME	INTRAFIELD	INTERFIELD	TIMING	USE
1	GDS	✓	✗	No Silicon needed	FeedForward
2	Scanner reports	✓	✓	Silicon / Lots	FeedBack
3	Focus maps	✓	✓	Silicon / Lots	FeedBack
4	Topography	On-going	Planned	Silicon / Lots	FeedForward & FeedBack
5	SSF	✓	✓	Silicon / Monitoring	FeedForward

## 7. Multivariate analysis

The Partial Least Square (PLS) regression analysis was chosen to investigate the correlations that exist between each of the previous datasets. PLS is a linear multivariate method.

GDS is the most predictive file that is available since it exists before any silicon is processed in the waferfab. It will be utilized as the x-input of each of the following analysis.

Scanner levelling data, focus maps and topography measurement were used as y-values in the regression tooling. Figure 5 gives a schematic view of the analysis process.

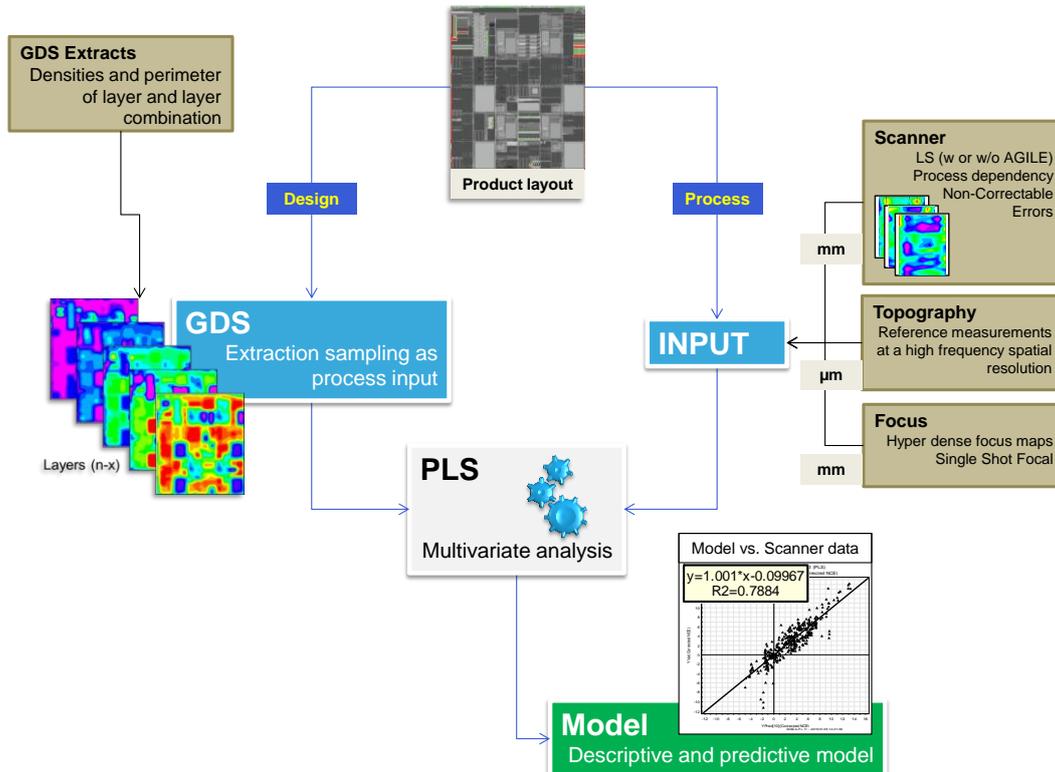


Figure 5: Schematic view of the process through PLS regression analysis

Two correlation parameters are calculated by the PLS analysis tooling.

- $R^2$  or goodness of fit of the model. It gives the description quality of the model.
- $Q^2$  or goodness of prediction. It is related to the capability of prediction that can be expected from the model.

The best model is the one with the best couple ( $R^2$ ,  $Q^2$ ).

Here the PLS is used to answer to the following question:

- Can scanner levelling data and topography be anticipated from design data? How does it relate to focus?

### III – GDS DESIGN DENSITY ANALYSIS INTRAFIELD LEVELLING PREDICTABILITY

The scanner levelling measurements are related to the product layout as described in chapter I.

If the levelling capabilities of the scanner could be predicted, it would be possible to anticipate the existence and the extent of the uncorrected parts of the chip.

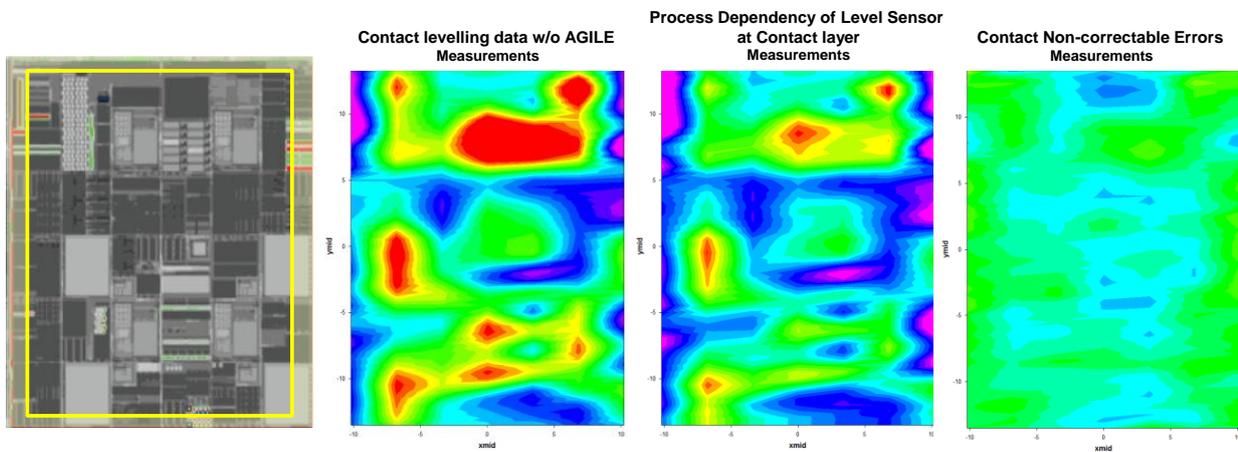


Figure 6: Scanner levelling reports vs. Product layout (the yellow box is the part of the chip that is being measured by the levelling system of the scanner). Visually, the shape of the levelling fingerprints seems to be related to the product layout.

The methodology consists of reconstructing what is on the wafer before the exposure step using all the previous layer design data from GDS's. Extractions were performed for every previous patterning layer. These may be single patterning, double patterning or the convolution of two layers that are expected to contribute to topography together. It can also be a perimeter density or a spatial density maps. All underlying layers were investigated but only the ones that showed correlation were kept.

As Figure 6 suggests, it seems that a correlation exists between the product layout and the levelling data of the scanner. The optimal underlying GDS density selection for achieving best possible correlation is shown in figure 7 for three 14FDSOI layers.

Due to the fact that it was expected to have more topography, the Contact layer has been specifically studied into more details. GDS extracted densities were used as X parameters for the model building and the 14FDSOI Contact layer scanner reports were set as the output of the modelling. Running the simulation several times, it was possible to select the best combination of GDS data and the layers with the most influence on topography, level sensor performances, levelling non-correctable errors. The same GDS inputs were used in all cases.

These results are presented in Figure 8. It shows the reconstructed intrafield levelling fingerprint using the modelled data versus the measurements as well as correlation plots and coefficients ( $R^2$  and  $Q^2$ ).

	X-inputs: GDS densities	Y-inputs: Scanner levelling reports for layer N		
	PREVIOUS LAYERS	TRENCH	CONTACT	METAL 1
Single layers input Density and Perimeter	Layer N-7	X	X	X
	Layer N-6	X	X	X
Convolutions of layers (double patterning, stack effects...) Density and Perimeter	Convolution 1	X	X	X
	Convolution 2	X	X	X
	Convolution 3	X	X	X
	Convolution 4		X	X
	Convolution 5			X

Figure 7: Underlying layers GDS densities used for correlating Trench, Contact and Metal 1 layers

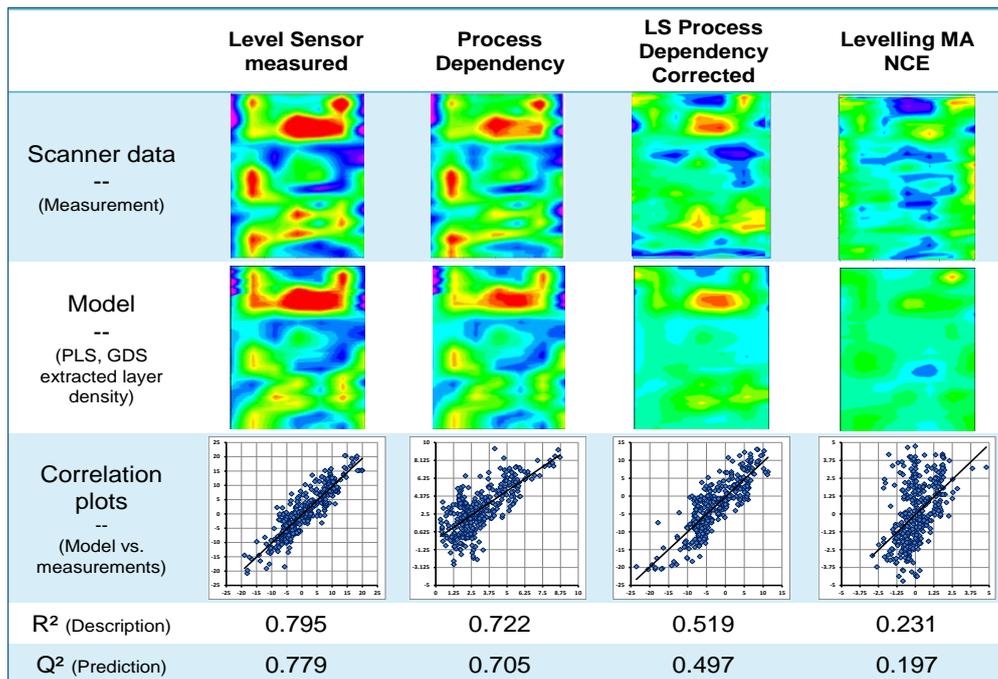


Figure 8: Measured and predicted levelling fingerprints; Correlation plots; description correlation coefficient R<sup>2</sup> and expected prediction capabilities Q<sup>2</sup> of the model for intrafield levelling data at Contact layer

## 1. Level Sensor without AGILE

For the level sensor alone, the model has a R<sup>2</sup> of 0.80 and a Q<sup>2</sup> of 0.78. This shows that the level sensor measurements have a high correlation to the stack densities. The next step is to check if this reading can be calculated beforehand using another maskset. The level sensor measurement is giving both topography measurements and a certain amount of optical modulation induced reading error. The two parts are explained in sections III.2 and III.3.

## 2. Process Dependency

The delta map between the LS and the LS with AGILE measurement contains process dependency of the LS. It is an indirect measurement of the optical modulation of the stack.

With the model, about 72% of this reading error can be explained and around 71% could be predicted. As shown in Figure 9, SOI (Silicon on Insulator) parts of the chip measure a lower topography compared to the rest of the field which

contains some No SOI, i.e. Bulk, zones. This can be explained simply by the presence of a reflective Silica layer in the SOI part. This layer explains about 50% of the reading errors.

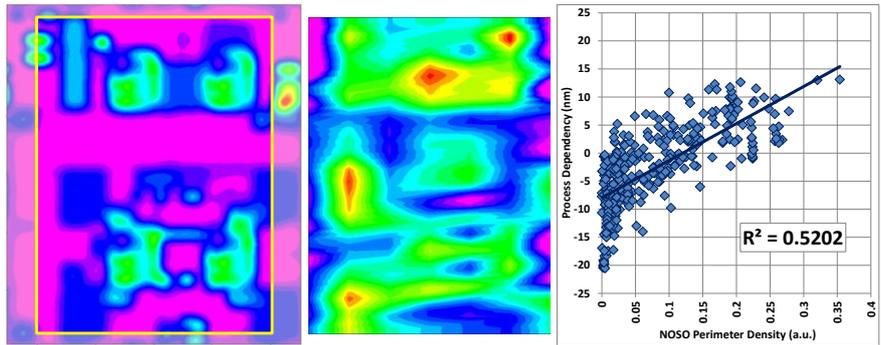


Figure 9: SOI/Bulk intrafield layer density (purple is SOI and blue and green are Bulk substrates, at the left) vs. scanner measured process dependency (middle) and correlation plot between the two (right).

Once again, the absence of trilayer planarization effects causes some error. Other processes such as CMP or doping could be added to the model in order to increase the correlation coefficients since these layers create different stacks that have different effects on the optical LS and may have an influence topography build-up.

### 3. Level Sensor Process Dependency corrected

Using the AGILE sensor, it is possible to extract the wafer topography without the process dependency error that may be present in the optical LS measurements.

The model shows a  $0.52R^2$  correlation to product layout and a prediction of around 50% can be expected applying the model to GDS extracted data. The correlation is lower than for the LS alone but this was expected since the material distribution induced optical modulation is not taken into account. The model also only considers the patterned material that is present on the wafer and the planarizing effects of the litho stack (trilayer) were not added to the modelling parameters. As expected, it is the previous layer (named Trench) that has the largest influence on the wafer topography at the Contact layer.

### 4. Levelling Non-Correctable Errors

Non-correctable errors do not show a strong correlation to the GDS density model ( $R^2 = 0.23$ ,  $Q^2 = 0.20$ ). This is expected since the non-correctable errors include the scanner levelling model (in which the exposure slit is fitted through the data) and the GDS design does not.

As a conclusion to part III, this model has been built on a specific maskset and has yet to be checked with another dataset. The model will be applied on the GDS densities of the new product and compared with real-life measurements (FEM, Levelling reports, topography) on silicon wafers.

## IV – 7 WAFER FEM ANALYSIS

In order to qualify on-product total focus uniformity performance, 7 product wafers were exposed with focus offsets in a range of +/-45 nm around best focus. Per full field 52 identical product features were measured by CD-SEM. For each of the almost 5000 points on the wafer the local defocus is fitted, as shown in Figure 10. A plot of the measured CD values as a function of focus setpoint plus local defocus shows the fit quality as the 'bandwidth' of points around the fitted Bossung shape; see Figure 11. The remaining bandwidth is the result of inevitable scanner wafer-to-wafer variation and SEM noise.

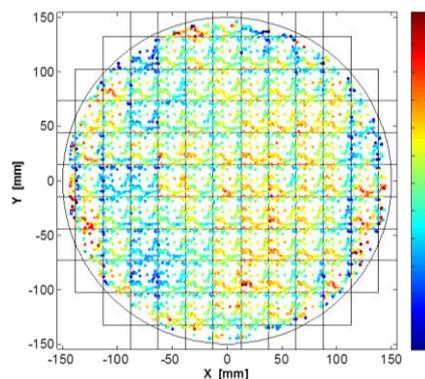


Figure 10: Defocus map obtained from multi wafer FEM; the estimated accuracy per point is around 3 nm 3 $\sigma$

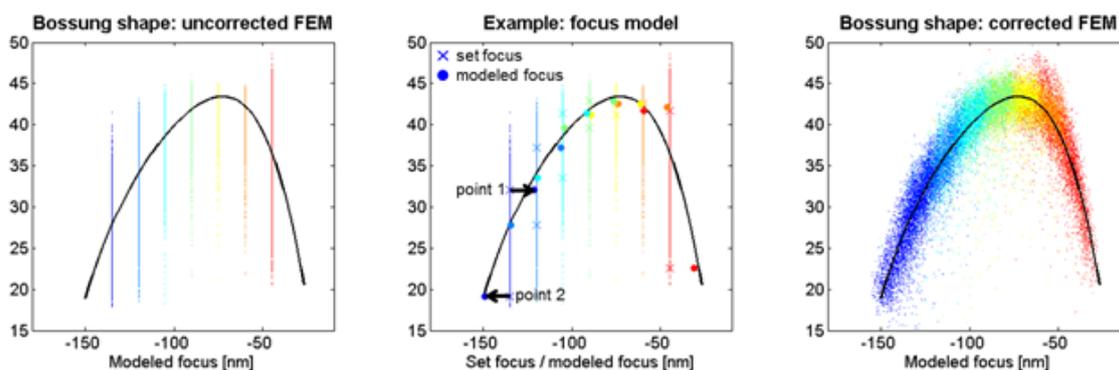


Figure 11: Bossung plot with corrected focus axis indicates regression quality. In the center graph the focus axis correction is shown for two points on the wafer. All 7 wafers (focus setpoints) belonging to that wafer point get shifted by the same modelled defocus.

Figure 12 shows the average field defocus map. All fields not too far to the edge are used for averaging. Levelling MAZ residual correction is applied.

In-die on-product focus measurement and control could be used to correct for the linear wedge (tilt over Y) component. For correction of the average X curvature, lens tuning is needed. Locally (between neighbouring points) no large focus offsets are seen, which could be because all measured points are in sub-scribes, where similar topography is expected.

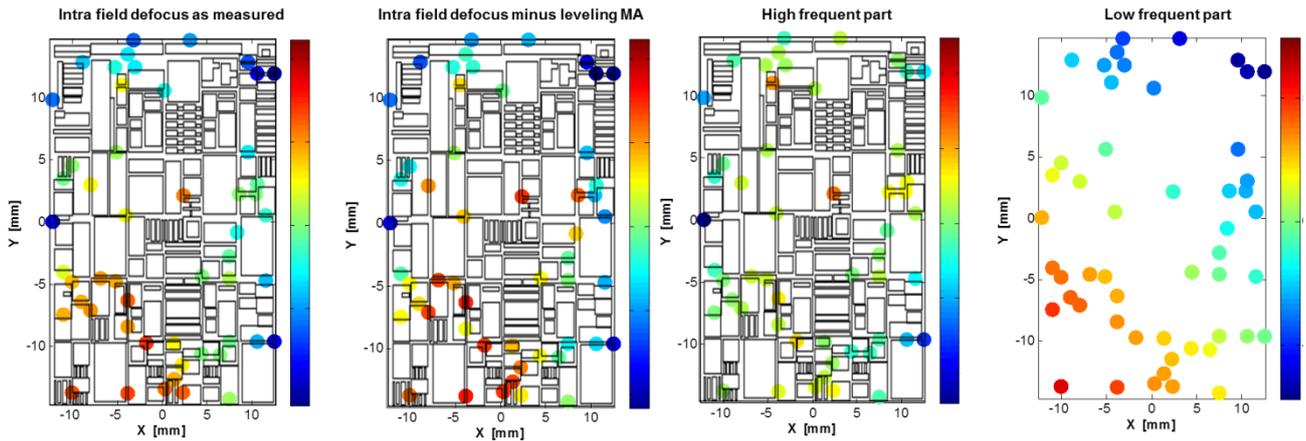


Figure 12: Measured intra field defocus map with and without leveling MA correction; the latter is also split into a low order shape and a spatially high frequent part (to be compared to topography measurements); the estimated accuracy per point is around  $2 \text{ nm } 3\sigma$

In Figure 13 we see that the on-product inter field defocus map contains global and more local components. The difference map contains a clear global shape. Spatially intermediate frequencies like field offsets are caught by both FEM and SSF. These frequencies do catch our eye, and that's why the resemblance between FEM and SSF seems so good. Actually around 50% of the on-product defocus variance measured by FEM is caught by the SSF measurement.

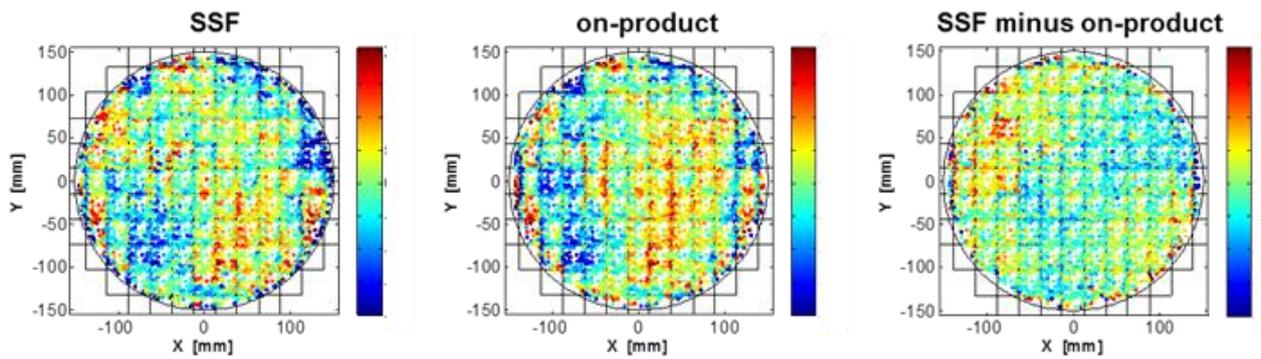


Figure 13: About 50% of the inter field focus variance seen by FEM is also seen by Single Shot Focal (SSF)

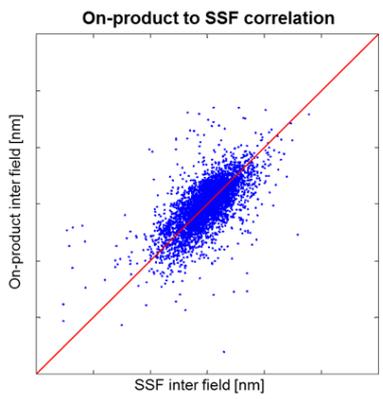


Figure 14: A correlation plot between FEM and SSF shows there is a shape difference ('cloud width'), but not scaling error ('cloud on red 1:1 line')

## CONCLUSION

Reticle design GDS maps show high ( $\sim 0.7 R^2$ ) correlation to, predominantly, level sensor raw data and level sensor process dependency. The next step would be to verify this correlation on another mask set. If correlation is seen this could be used to feedforward focus and levelling optimization, improve FEM strategies and die layout optimization. To lesser extent a correlation ( $\sim 0.5 R^2$ ) is seen to wafer topography measured by the scanner level sensor. Further work is ongoing to improve the correlation by measuring micrometre scale topography maps using offline optical tooling. This correlation, also, needs to be verified on another mask set. A strong visual correlation is seen between SSF and on-product focus fingerprints and about 50% of the variance seen by 7-wafer FEM are also seen by Single Shot Focal (SSF). This indicates that SSF can be used to give a good representation of interfield focus uniformity seen at wafer level. The intrafield on-product focus is dominated by a lower order fingerprint. This can be further corrected by the scanner using wafer tilts. The higher order topography effects are not dominant in this measurement because of the choice of measurement features. Further work can be done by measuring features within the product and the sub-scribes together.

This paper has shown correlations between level sensor and reticle design GDS. The next step will be to investigate correlation between on-product focus and topography measurements, and close the circle by confirming the correlation with reticle design GDS maps.

The layout dependent local topography investigation in this paper is also linked to focus induced defectivity. The defect detection and control of this is covered in the paper and talk: A new paradigm for inline detection and control of patterning defects [8].

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