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Verification and application of multi-source focus quantification

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Abstract:

The concept of the multi-source focus correlation method was presented in 2015 [1, 2]. A more accurate understanding of real on-product focus can be obtained by gathering information from different sectors: design, scanner short loop monitoring, scanner leveling, on-product focus and topography.

This work will show that chip topography can be predicted from reticle density and perimeter density data, including experimental proof.Different pixel sizes are used to perform the correlation in-line with the minimum resolution, correlation length of CMP effects and the spot size of the scanner level sensor.Potential applications of the topography determination will be evaluated, includingoptimizing scanner leveling by ignoring non-critical parts of the field, and without the need for time-consuming offline topography measurements.
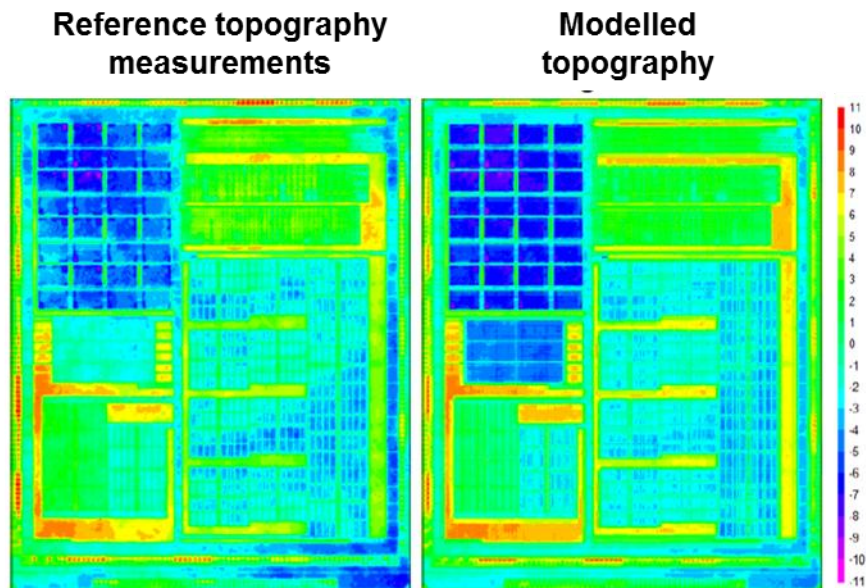
Fig 1: High resolution topography (Left: Measured; Right: Simulated) – Colour scale is in nm

KEYWORDS:
Depth of focus, intrafield, scanner leveling, topography, scanner, product design layout effect, PLS regression analysis

INTRODUCTION

The concept of the multi-source focus correlation method was presented in 2015 [1, 2]. A more accurate understanding of real on-product focus can be obtained by gathering information from different sectors: design, scanner short loop monitoring, scanner leveling, on-product focus and topography. In reference [1], the link between scanner monitoring and on-product focus was established as well as the correlation between design and the scanner level sensor measured intra fieldnon-correctable errors after leveling. In [2], the on-product focus to topography correlation has been studied and the concept of smart leveling was proposed.

This work will investigate the design to topography and design to focus correlation. It has been shown that chip topography can be predicted from reticle density and perimeter density data, including experimental proof. To visualize the potential applications different pixel sizes will be used to perform the correlation in-line with (i) minimum resolution, (ii) correlation length of Chemical Mechanical Polishing (CMP) effects and (iii) scanner level sensor spot size. Potential applications of the topography determination will be evaluated, including optimizing scanner leveling by ignoring non-critical parts of the field.

I – INTRAFIELD FOCUS CONTROL

Best focus variation, coupled with reduced depth of focus, is a major contribution to tight process margins for the 28nm and 14nm logic nodes.For both intra wafer and intra field, process and tool fingerprints are creating local shifts from the best focus, causing printing issues leading to defectivity and yield losses.

Major contributors to interfield focus arescanner fingerprints [1], edge effects [7] and leveling non-correctable of the wafer topography [2, 3, 4,and 5].

Considering theintrafield, it is possible to distinguish two families of effects: the imaging effects and the spatial effects, summarized in Fig.2. From imaging, the best focus shift is caused by wave front deformations induced in a large part by the light passing through the mask so that the image focal plane of each pattern shift apart from each other making it more difficult to print [6]. Best focus is pattern shape dependant.

Spatial effects are characterized by a best focus change across field for the same pattern. The mask is not perfect and the same pattern may not have been printed exactly the same way for each of its occurrences. Imaging effects (i.e. image plane deviation measured by FOCAL) can also effect the BF of a single pattern differently across the field [15]. The wafer topography also has an intrafield component showing non-correctable systematics that are tightly linked to the on-product focus [2]. For a given pattern, best focus depends on the intrafield position of each of its occurrences across field. This part of the intrafield focus budget is the one studied in this paper.
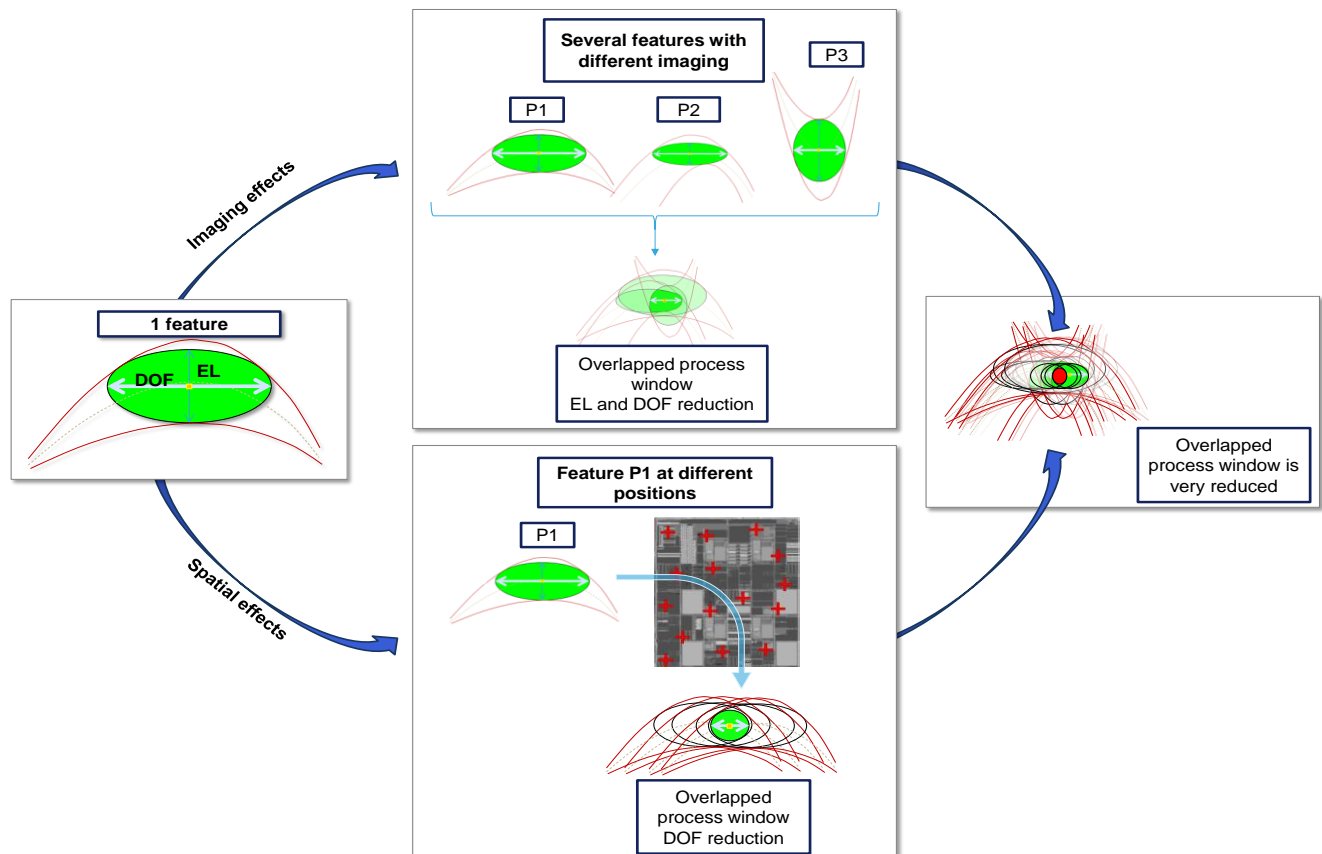

Figure 2: Brief overview of some of the sources of intrafied focus variability

II – THE TOPOGRAPHY INDUCED FOCUS NON-UNIFORMITY

As written above, focus is a function of the pattern and its position. It has been shown in reference [2] that focus distribution is mainly topography driven. Fig. 3 shows two things that can be derived from offline reference topography measurement done on a Veeco WYKO NT9300 tool in LETI without the photolithography process stack [8]. The height distribution in field (in green) which is mainly spread between 45 and 75nm but presents some excursions of a few tens of nanometres in atypical areas of the chip and the best focus to topography correlation (in blue) which shows a slope close to 1with an excellent correlation factor.
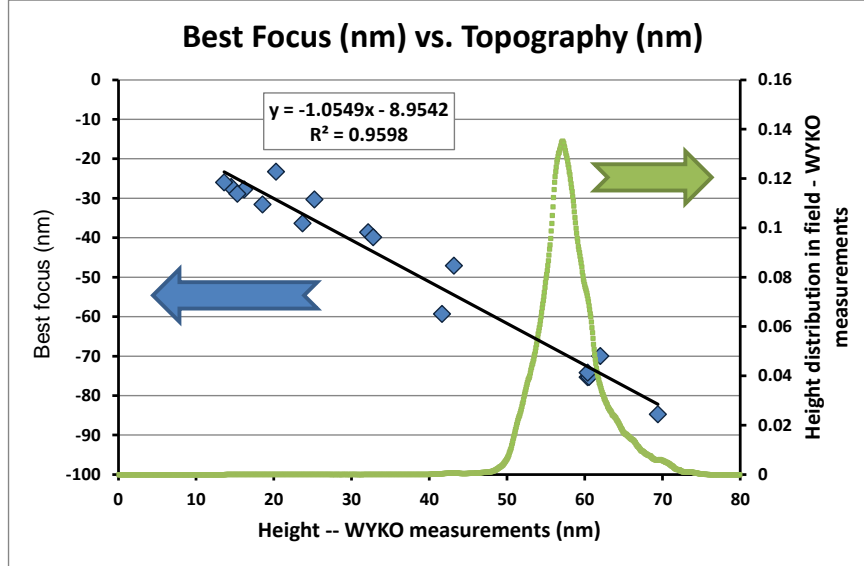

Figure 3: Correlation plot showing Bossung tops determined on-product focus vs. Local topography measured by a Veeco WYKO NT9300 tool and height distribution through chip.

A correlation was seen with the level sensor measured intrafield height map (with and without process dependency error corrected) andintra fieldleveling non-correctable errors. Process dependency is a measurement error due to optical stack effects on the older generationlevelsensor, and it is corrected by the AGILE Sensor. The PLS gives the Q² parameter thatindicates how well a variable can be predicted. Level sensor measured intrafield height map and process dependency corrected map showed respectively 0.78Q² and 0.50Q² expected prediction capabilities.

As one aspect ofleveling is a measurement of the topography of the wafer, it is expected that the PLS coefficients w_j can be calculated for reference topography as well:

$$Topography_{Wyko\ Measured} = \sum_j (w_j LAYER\_DENSITY_j) (2)$$

Intrafield wafer topography is layout driven. Each part of the chip has a specific design linked to its electrical behaviour (logic cells, memory cells, electrical protection, analogic devices, antennas, etc.) which all have their specific design, dimensions and densities. This variety of different devices can create some local topography induced by patterning and polishing steps.Some tiling is done within the chip to homogenize the density and mitigate those effects but it is not always sufficient. As a consequence, the assembly of a chip within a mask field will lead to a specific topological map. Fig. 4 illustrates this fact by showing an example of 14FDSOI (Fully depleted silicon on insulator 14nm technology node) test chip shuttle and the topography measured at the Contact layer.
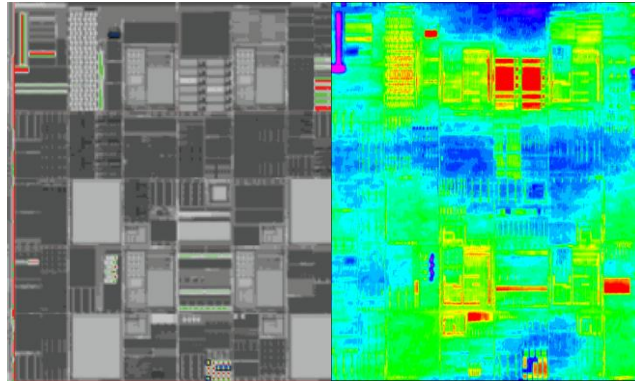
Figure 4: Product layout of the 14FDSOI test chip shuttle and topography measured on a complete field before Contact exposure

Consequently, it is possible to create a predictive model of the intrafield topography using the GDS of the product as an input.

III –MODELLING TOPOGRAPHY WITH GDS DENSITIES

In this paper, the same methodology as the one described above (in part II) and in the SPIE 2015 paper [1] was applied in order to link the GDS to offline topography measurements. These were done on a VeecoWYKO NT9300 tool in LETI without the photolithography process stack [8]. A topography model was constructed using apartial least square linear prediction method by combining GDS densities of the underlying layers.Differentmodels were investigated with different pixel sizes to be sensitive to several effects at multiple ranges.

- Short range effects

These effects are the ones thatbetter match the capabilities of the Wyko in terms of spatial resolution. They are related to the direct impact of the design on a localized area.

- Long range effects

These effects are mainly process induced (deposition uniformities, CMP dishing, loading effects on etch). Some layout effects such as assembly can be responsible for these by creating areas with different designs and densities.

The PLS coefficientsfor each effect were calculated on a small part of the chip for 14FDSOI Contact layer and then testedon a larger area of the field containing about 800 times more data points for validation.

This first graph (see Fig. 5) shows the comparison between the expected performance of the model regarding prediction capabilities Q^2 and the actual performances by the model R^2_{test}, for each of the pixel sizes chosen in this study.
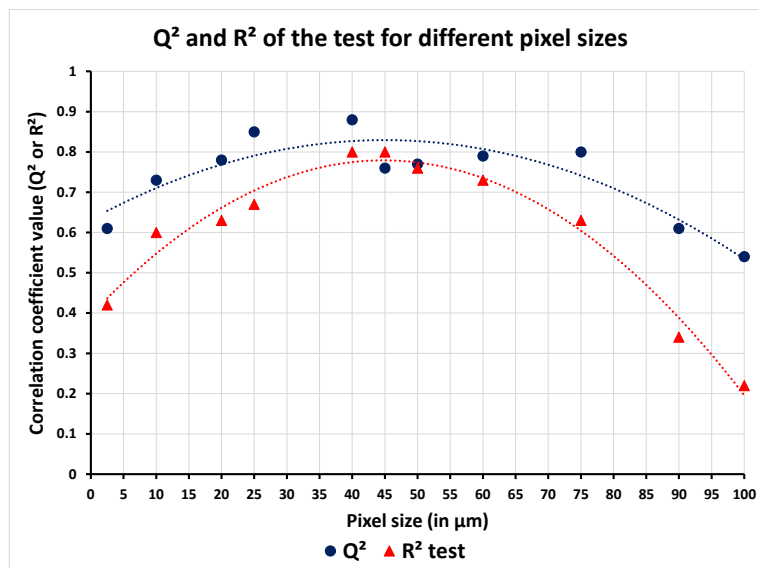

Figure 5: Graph comparing Q^2 and R^2_{test} values for several pixel sizes

The optimum model comes with pixel sizes of 40 to 50µm.Theseshowed the best description and expected prediction capabilities of the topographyand the best results after testing on a larger area. In order to elect the optimal pixel size, it is necessary to look at other data given by the PLS model such as the predicted range of the values. A model can have a high correlation coefficient and still gives values that are not representative of measured topography. The closer the slope between measurement data and predicted data is to 1, the better the model is representative of the wafer actual topography. The following figure, Fig. 6, gives the detailed results for the some of the best test cases. It compares model build-up, expected performances vs. actual performance (correlation coefficient, slope) and mappings of the data.

The slope of the correlation plot between measurement and model data is never exactly equal to 1. This can be explained by the fact that the models used in this work are empirical and based on theextraction of the density data at a given pixel size and also because the measurement data is also averaged to the same resolution to perform the validation of the results. This averaging, especially with large pixels, will induce a reduction of the total range of heights since highest peaks and lowest valleys are smoothened by the data averaging.

This second dataset shows best performing models to be the 40 and 45µm-pixel ones. The model parameters were calculated without full use of the PLS analysis capabilities. This statistical method gives not only model coefficients and prediction capabilities forecast but also a ranking of the importance of each input by evaluating the VIP (Variable Importance in the Projection) of every component [12, 13]. This VIP gives the components that are actually discriminating in the regression – in this case, the layers that will have a substantial influence in the topography built-up.
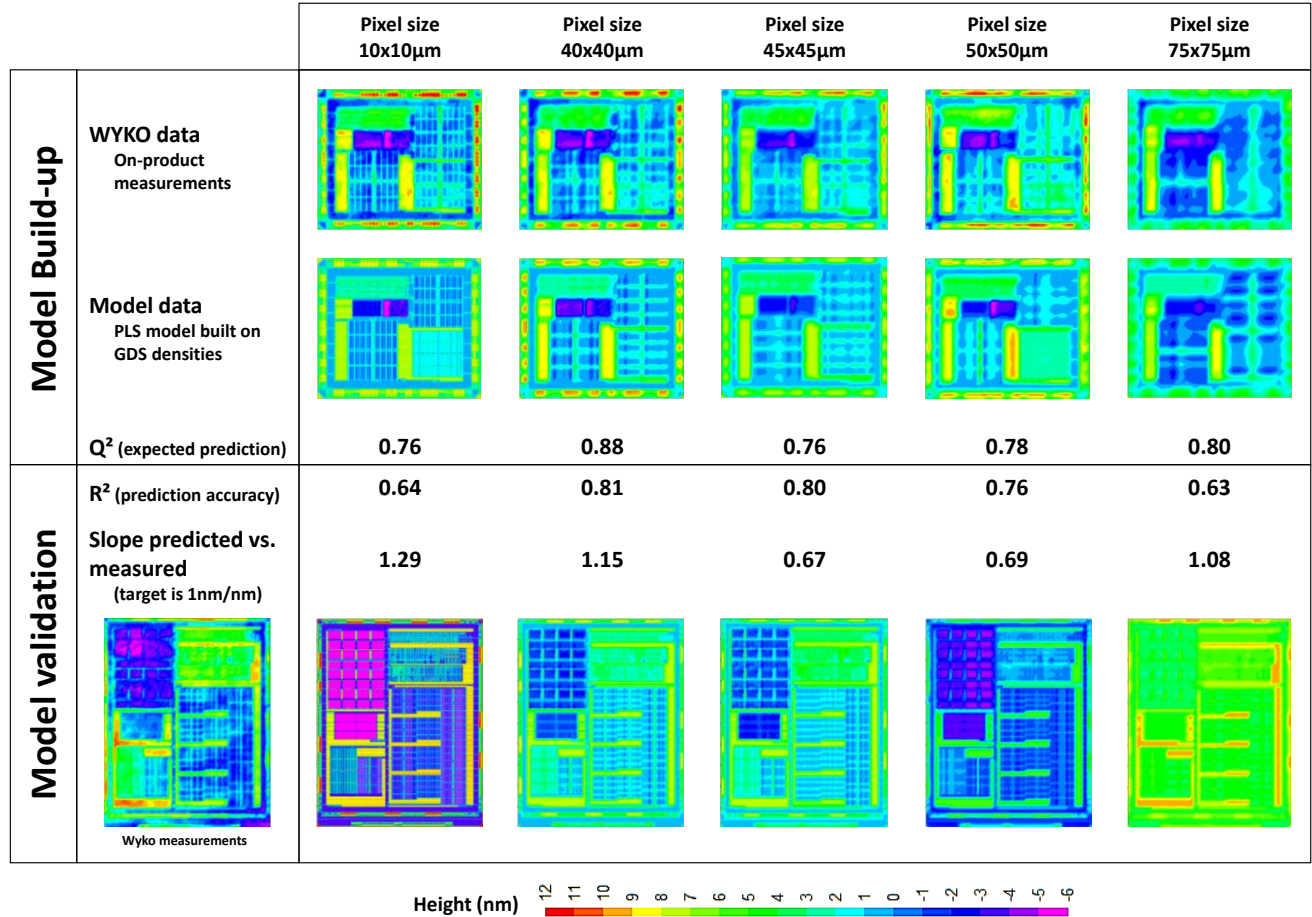
		Pixel size 10x10µm	Pixel size 40x40µm	Pixel size 45x45µm	Pixel size 50x50µm	Pixel size 75x75µm
Model Build-up	**WYKO data** On-product measurements					
	Model data PLS model built on GDS densities					
	Q² (expected prediction)	0.76	0.88	0.76	0.78	0.80
Model validation	**R² (prediction accuracy)**	0.64	0.81	0.80	0.76	0.63
	Slope predicted vs. measured (target is 1nm/nm)	1.29	1.15	0.67	0.69	1.08
	Wyko measurements					

Height (nm) 12 11 10 9 8 7 6 5 4 3 2 1 0 -1 -2 -3 -4 -5 -6

Figure 6: Performances of a few models for topography prediction

→ Model build-up (~3mm²): R² shows the data description capability and Q² the data expected prediction capability of the model

→ Model application on a larger area (20mm²) is compared to high frequency measurement data

It has been show above that the topography could be predicted using a linear combination of layer densities and perimeters determined by PLS analysis. As the focus is related to the local height by a linear relation since most of these high spatially frequent topography are scanner leveling non-correctable, local defocus can be predicted through this modelling. Combining relation (2) and the trend line given by Fig. 2 gives:

$$\begin{cases} Topography = \sum_j(w_j\,LAYER_{DENSITY\,j}) \\ Best\ Focus = (-1)*Topography + b \end{cases} \Leftrightarrow \quad Best\ Focus = (-1)*\sum_j(w_j\,LAYER\_DENSITY_j) + b \qquad (3)$$

This prediction enables the definition of care areas i.e. areas in which critical patterns in terms of imaging, determined by full chip LMC [9, 10], and high local topography variation might be found, causing high probability of patterning failure.The capability of defining smart care areas is key for process improvement efficiency.Using the VIP information as an input to the design may allow an improvement of the dummification process and chip layout.Simulated topography can also serve as an input for Process Window Optimizer (PWO) but for control plan optimisation by giving care areas to be monitored. It can also be used as an input for a smart scanner leveling capable of correcting preferentially the topography where it matters.This last solution was investigated in this work and is discussed in the next section of the paper.

IV – FOCUS CONTROL THROUGH SCANNER LEVELING OPTIMIZATION

High-resolutionintrafield topography modelled from the design layout density can be a useful source to tailor scanner leveling for optimizing the focus control within the care area. Scanner leveling can be referred to as the process of correctly positioning the fields of the wafer in (best) focus during exposure.Levelingis limited by, among others, the physical shape of the exposure slit of the scanner. In the following paragraphs, we proposed a scheme for care and ignored area driven leveling.
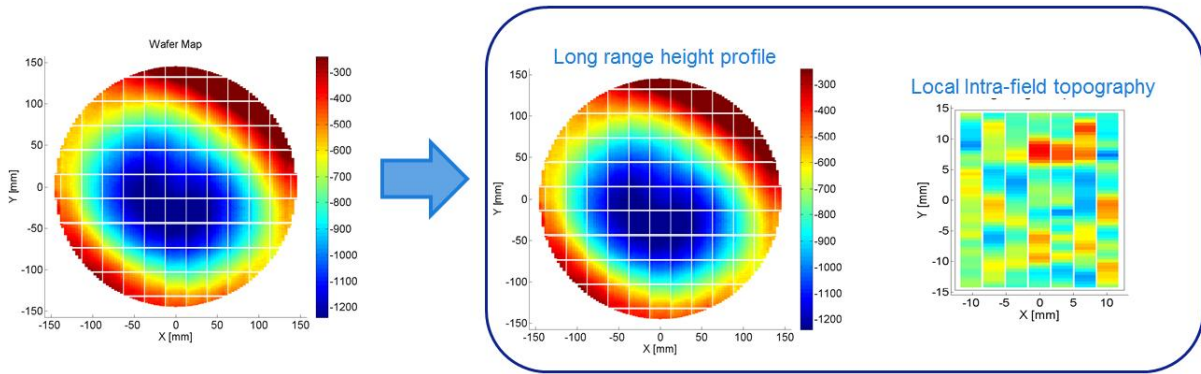

Figure 7: Wafer height map decomposed into long range height profile and local intrafield topography.

Levelinguses scanner level sensor measured surface height information of the chucked wafer, known by 'wafer map', as input. Figure 7 shows a wafer mapwhichcontains multiple areas corresponding to dies or fieldsA full wafer map can be decomposed into two parts; a long range height profile (inter field) that represents the global shape of the wafer and a local (intrafield) height map that is sufficiently repetitive among fields. These two parts can be processed separately by the leveling algorithm, and then algebracally summed to generate the wafer stage positioning setpoints. Additionally, in our previous communication [1], and sections above, we showed that layout design density modelled topography map reasonably correlate with the level sensor measured local intrafield topography or even high-resolution topography measurement with external tools(e.g. Wyko). Consequently, we can substitute this local intra-field height map with the intra-field modeled topography map. Thanks to its high resolution, it will allow us to define accurately the care and ignore area and thus,to enable their preferential treatment in leveling for better focus control.

In figure 8 (left), some areas within the field are highlighted as care (green), ignore (red), and non-specific (orange) area. These areas areidentified based on the process and design knowledge. However, they can also be identified using other computational lithography products. These defined areas are then mapped into the dense intra-field topography in figure 8 (right). Although we can, in principle, use the modelled intrafield topography, we used the external tool measured topography in this example since modelled topography was not available for the full field.
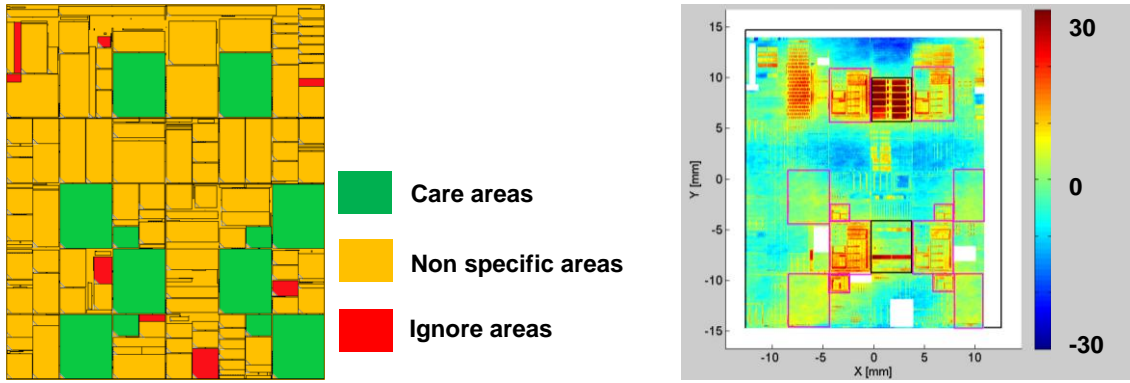
Figure 8: Care (green), ignore(red), non-specific (orange) area are highlighted on the design layout (left). Care and ignore area are then mapped into the intrafield topography (right). In right figure, height values of the ignore areas are removed (white) and care area are given higher emphasis and marked with rectangles.

A modified (weighted) scanner leveling algorithm was applied offline to this care-and-ignore area mapped intrafield topography. The non-correctable errors at care area after such leveling are reduced leading to improved focus control. Figure 9 compares (delta) the non-correctable error after the dense topography-assisted, care-and-ignore area driven leveling and the standard (all area are equally weighted) leveling. Positive (red) values show improvement. Figure 9 shows care area improved (upto 9nm in some area) with a tradeoff deterioration at the non-specific or ignore area. Figure 9 (right) shows the cumulative distribution of the non-correctable error samples (points) within the field. Within the care area, 3% more samples are now in the spec (15nm) without pushing any locations within the non-specific or ignore area beyond their spec (25nm). Spec for the non-specific/ignorearea is larger than that of the care area. Note, although the choice of the spec values in this example isarbitrary, they are representative for this process. Further optimization can lead to larger improvement in the care area.
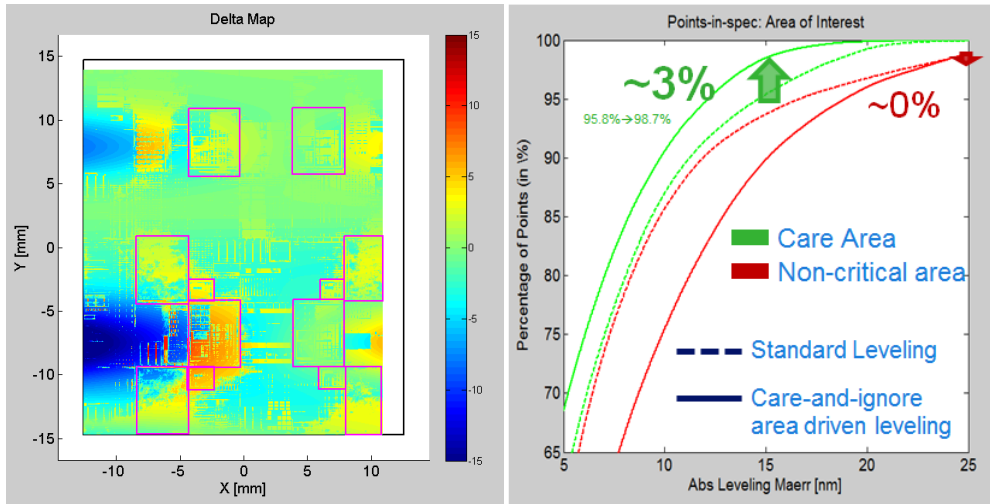

Figure 9: (left) Delta map of the non-correctable errors from care-and-ignore area driven leveling and the standard leveling. A positive value means improvement. The right figure shows cumulative distribution of the leveling non-correctable error.

Note, this proposed technique is not currently available in the scanner. Therefore, we also discussed a possibility to achieve similar performance in the scanner by a feed-forward correction mechanismexploitingthe sub-recipe interface of the scanner. The delta between the care-and-ignore area optimized leveling and the standard one can be applied to the scanner through the feed-forward interface after converting them into a correction format suitable for that interface. This dense topography assisted care-and-ignore driven leveling can be used to find optimal configurations of scanner leveling improving edge die focus [14].
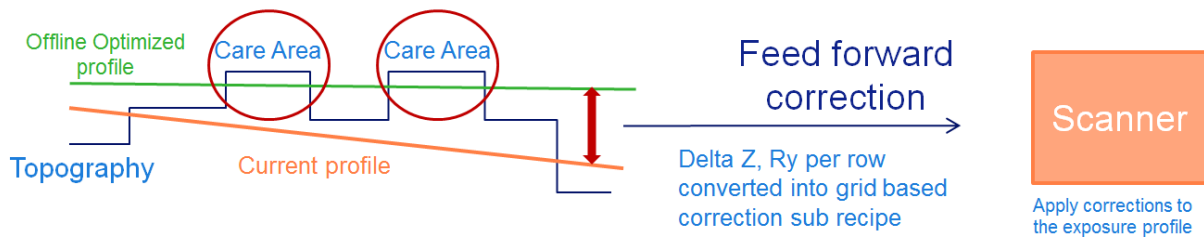
Figure 10: A schematic representation showing the possibility to enable care-and-ignore area based optimization through scanner's subrecipe interface feed forward subrecipe correction interface.

CONCLUSION

Topography measurements have been modelled and predicted with the Partial Least Square methodology with a high predictability capability up to $0.8Q^2$. The topography being a cause of focus intrafield excursions, this method allows the definition of care areas where focus margin will be reduced and defectivity may occur at a higher rate. The use of this data as an input for PWO [9, 10] will allow an improved defect prediction. The care areas were also used as an input for a smart leveling methodology where the scanner will correct preferentially the critical areas of the chip. Some other applications of the topography data, modelled or measured, would be tiling optimization and securing the reticle assembly.

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